Texas Instruments Advanced Product Information

SN76115N

Stereo Demodulator

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FEATURING

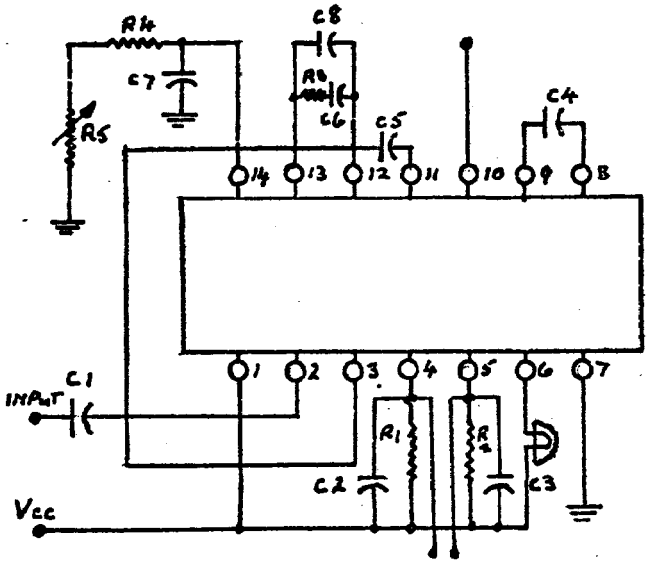
* REQUIRES NO INDUCTORS
* LOW EXTERNAL PART COUNT
* ONLY OSCILLATOR FREQUENCY ADJUSTMENT NECESSARY
* INTEGRAL STEREO/MONAURAL SWITCH 75 mA LAMP DRIVING CAPABILITY
* WIDE DYNAMIC RANGE: 560 mV (RMS) MAXIMUM COMPOSITE INPUT SIGNAL
* WIDE SUPPLY RANGE: 8-16 Vdc
* EXCELLENT CHANNEL SEPARATION MAINTAINED OVER ENTIRE AUDIO FREQUENCY RANGE
* LOW DISTORTION: TYPICALLY 0.3 THD AT 560 mV (RMS) COMPOSITE INPUT SIGNAL
* EXCELLENT SCA REJECTION

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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

RATING	VALUE	UNIT
Power Supply Voltage	16	Volts
Lamp Current (Nominal Rating 12V Lamp)	75	mA
Power Dissipation (Package Limitation) Derate above T_A = +25°C	625 5.0	mW mW/°C
Operating Temperature Range (Ambient)	-30to+85	°C
Storage Temperature Range	-65to+150	°C

FIGURE 1 - TYPICAL APPLICATION



Parts List

C_1 = 2.0 uF
C_2 = 0.02 uF
C_3 = 0.02 uF
C_4 = 0.25 uF
C_5 = 0.05 uF
C_6 = 0.5 uF
C_7 = 470 pF
C_8 = 0.25 uF
R_1 = 3.9 k
R_2 = 3.9 k
R_3 = 1.0 k
R_4 = 16 k
R_5 = ~~5.0 k~~ 10 k

PIN FUNCTIONING

Pin 1 = V_{CC}
Pin 2 = Input
Pin 3 = Amplifier Output
Pin 4 = Left Channel Output
Pin 5 = Right Channel Output
Pin 6 = Lamp Indicator
Pin 7 = Ground
Pin 8 = Switch Filter
Pin ° = Switch Filter
Pin 10 = 19 kHz Output
Pin 11 = Modulator Input
Pin 12 = Loop Filter
Pin 13 = Loop Filter
Pin 14 = Oscillator RC Network

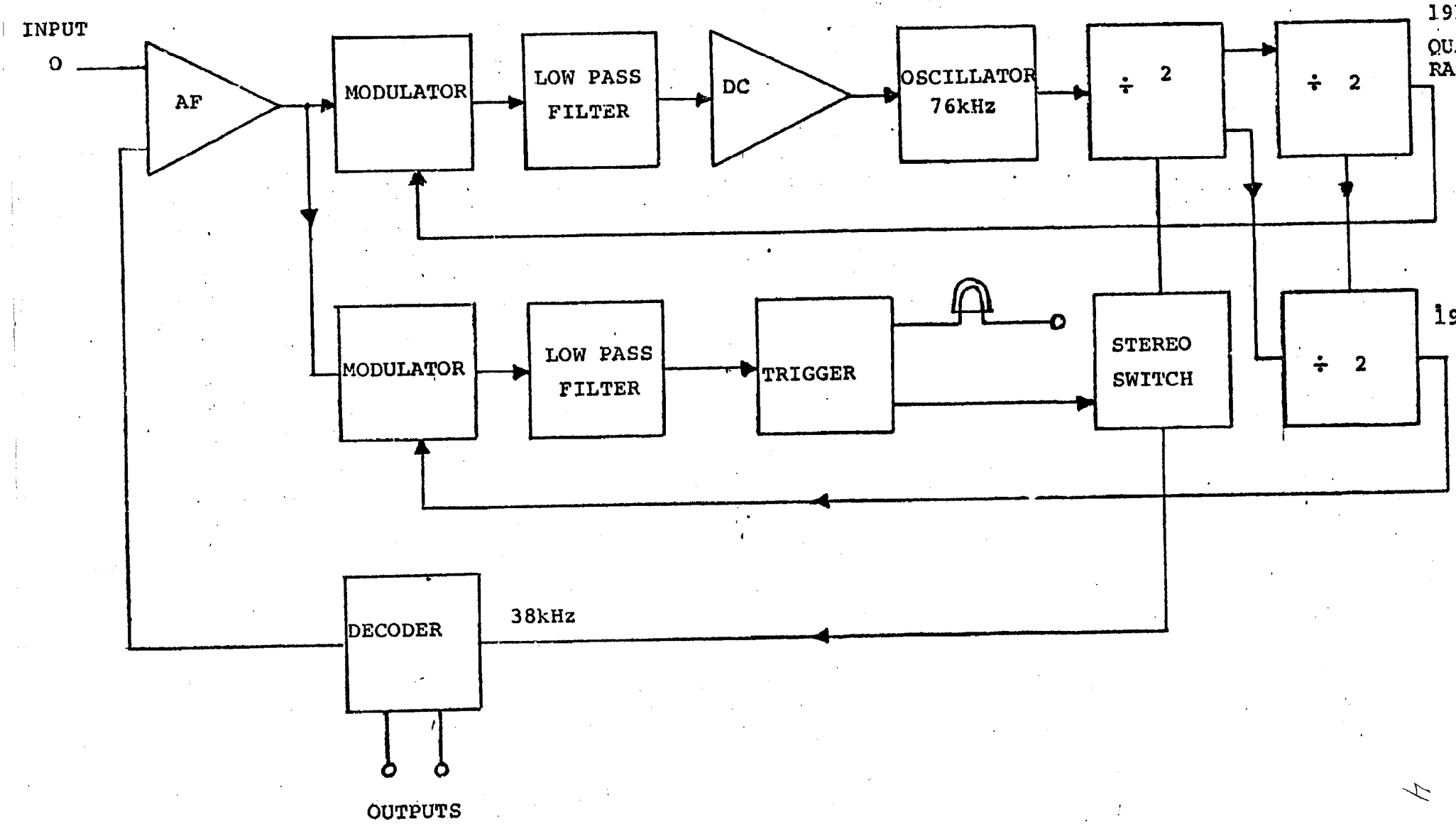
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ELECTRICAL CHARACTERISTICS Unless otherwise noted, V_{CC}* = 12 Vdc, T_A = +25°c, 560 mV(RMS) (2.8 Vp-p) standard multiplex composite signal with L or R channel only modulated at 1.0kHz and with 100 mV(RMS) (10%) pilot level, using circuit of Figure 1.

	Min	Typ	Max	Unit
Maximum Standard Composit Input Signal (0.5% THD)	2.8	-	-	V p-p
Input Impedance	-	50	[illegible]	k
Maximum Monaural Input Signal (1.0% THD)	2.8	-	-	Vp-p
Stereo Channel Separation (50 Hz - 15kHz)	30	40	-	dB
Audio Output Voltage (desired channel)	-	485	-	mV(RMS)
Monaural Channel Balance (pilot tone 'off)	-	-	1.5	dB
Total Harmonic Distortion	-	0.3	-	%
Ultrasonic Frequency Rejection 19kHz 38kHz	- -	34.4 45	- -	dB
Inherent SC A Rejection (f = 67 kHz;9.0 kHz beat note measured with 1.0 kHz modulation 'off)	-	80	-	dB
Stereo (19 kHz input level for lamp 'on) Hysteresis	12 -	16 6.0	20 -	mV(RMS) dB
Capture Range (permissable tuning error of internal oscillator, reference circuit values of Figure 1)	-	±3.0	-	%
Operation Supply Voltage (loads reduced to 2.7k for 8.0 volt operation)	8.0	-	16	Vdc
Current Drain (lamp 'off')	-	13	[illegible]	mAdc

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FIGURE 2 SYSTEM BLOCK DIAGRAM



CIRCUIT OPERATION

Figure 2, on the previous page, shows the system block diagram. The upper line, comprising the 38-kHz regeneration loop operates as follows:

The internal oscillator running at 76kHz and feeding through two divider stages returns a 19 kHz signal to the input modulator. There the returned signal is multiplied with the incoming signal so that when a 19kHz pilot tone is received a dc component is extracted by the low pass filter and used to control the frequency of the internal oscillator which consequently becomes phase- locked to the pilot tone. With the oscillator phase locked to the pilot the 38kHz output from the first divider is in the correct phase for decoding a stereo signal. The decoder is essentially another modulator in which the incoming signal is multiplied by the regenerated 38-kHz signal. The regenerated 38kHz signal is fed to the stereo decoder via an internal stereo switch. The stereo switch closes when a sufficiently large 19kHz pilot tone is received. The pilot tone level is detected and the switch operated by the stereo switch section of the circuit in the following manner :

The 19kHz signal returned to the 38kHz regeneration loop modulator is in quadrature with the 19kHz pilot tone when the loop is locked. With a third divider state appropriately connected, a 19 kHz signal in phase with the pilot tone is generated. This is multiplied with the incoming signal in the stereo switch modulator yielding a dc component proportional to the pilot tone amplitude. This component after filtering is applied to the trigger circuit which activates both the sterec switch and an indicator lamp.

APPLICATIONS INFORMATION

(Component numbers refer to Figure 1)

EXTERNAL COMPONENT FUNCTIONS AND VALUES

C_1 Input coupling capacitor- 1.0 uF is recommended but a lower value is permissible if reduced separation at low frequencies is acceptable.

R_1, R_2, C_2, C_3 Loads and de-emphasis capacitors, maximum permissible load resistors are related to minimum supply voltage as follows:

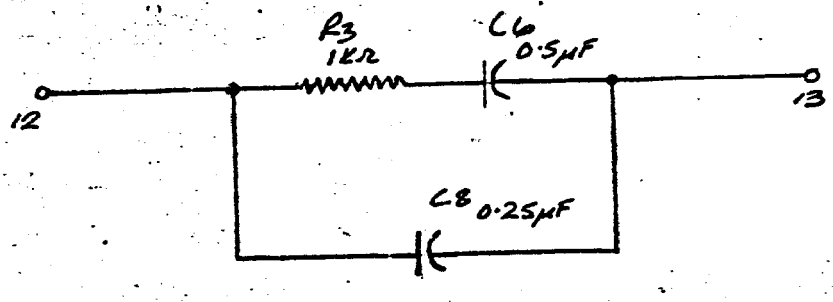
Min Supply	8.0	10	12	volts
Max Load	2.7	4.5	6.2	kilohoms

(± 10% Tolerance)

C_4 Filter capacitor for stereo switch level detector- time constant is C4 x 53 kilohms ± 30% maximum dc voltage appearing across C_4 is 0.25 V (pin 8 positive) at 100mV(RMS) pilot level. The signal voltage across C4 is negligible.

C_5 Internal coupling capacitor to modulators 0.05 uF is recommended. This gives 1.75° phase lead at 19Hz.

R_3, C_6, C_8 Phase lock loop filter components- the following network is recommended :



When less performance is required a simpler network consisting of R_3 = 100 ohms and C_6 = 0.25uF may be used (omit C8).

R_4, R_5, C_7 Oscillator timing network, recommended values :

C_7	=	470 pF	1%
R_4	=	16k	1%
R_5	=	5k	Preset

These values give ±3% typical capture range. Capture range may be increased by reducing C_7 and increasing R_4, R_5 proportionally but at the cost of increased beat-note distortion (due to oscillator phase jitter) at high-signal levels.

Stereo Lamp Nominal rating up to 75mA at 12v- the circuit includes surge limiting which restricts cold-lamp current to approximately 250mA.

19kHz-Output A buffered output providing a 3.0VpK positive-going square wave at 19kHz is available at pin 10. A frequency counter may be connected to this point to measure the oscillator free-running frequency for alignment.

External Monaural/Stereo Switching The circuit can be maintained in monaural mode by connecting pin 8 negative or pin 9 positive by 0.3V. Pin 8 may be grounded directly if desired. The dc impedance at pins 8 and 9 is 28 kilohms ±30%. Note that the voltage across C_4 increases to 2.2V with pin 9 positive when pin 8 is grounded.

Oscillator Killing In AM-FM receivers it may be desirable to kill the 76-kHz internal oscillator during AM reception to prevent interference. This may be accomplished by either grounding pin 14 or by connecting it to the positive line via a current limiting resistor (3.3 kilohms is recommended)

Phase Compensation Phase-shifts in the circuit cause the regenerated 38kHz sub-carrier to lead the original 38kHz by approximately 2°. The coupling capacitor C_5 generates an additional lead of 3.5° (for C_5 = 0.05 uF) giving a total lead of 5.5°.

It may be desirable that the regenerated 38kHz lead or lag the original to compensate for receiver IF characteristics.

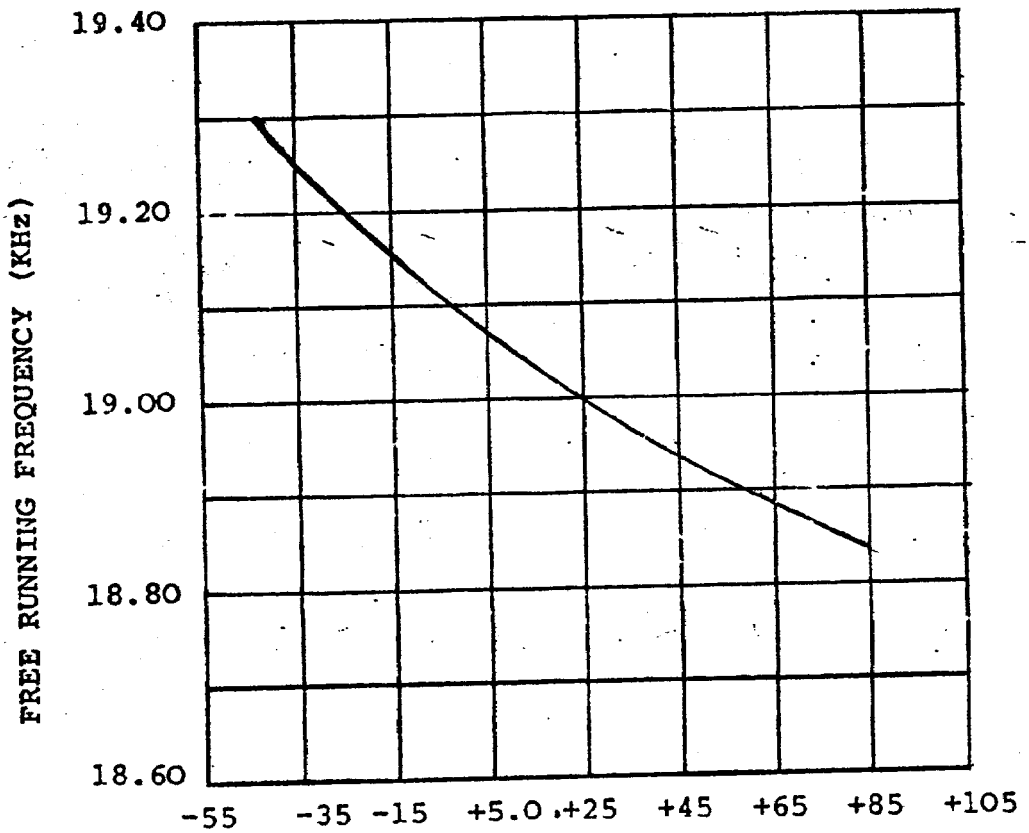
Further phase lead can be obtained if required by reducing C_5, which couples into a 5.0 kilohm load.

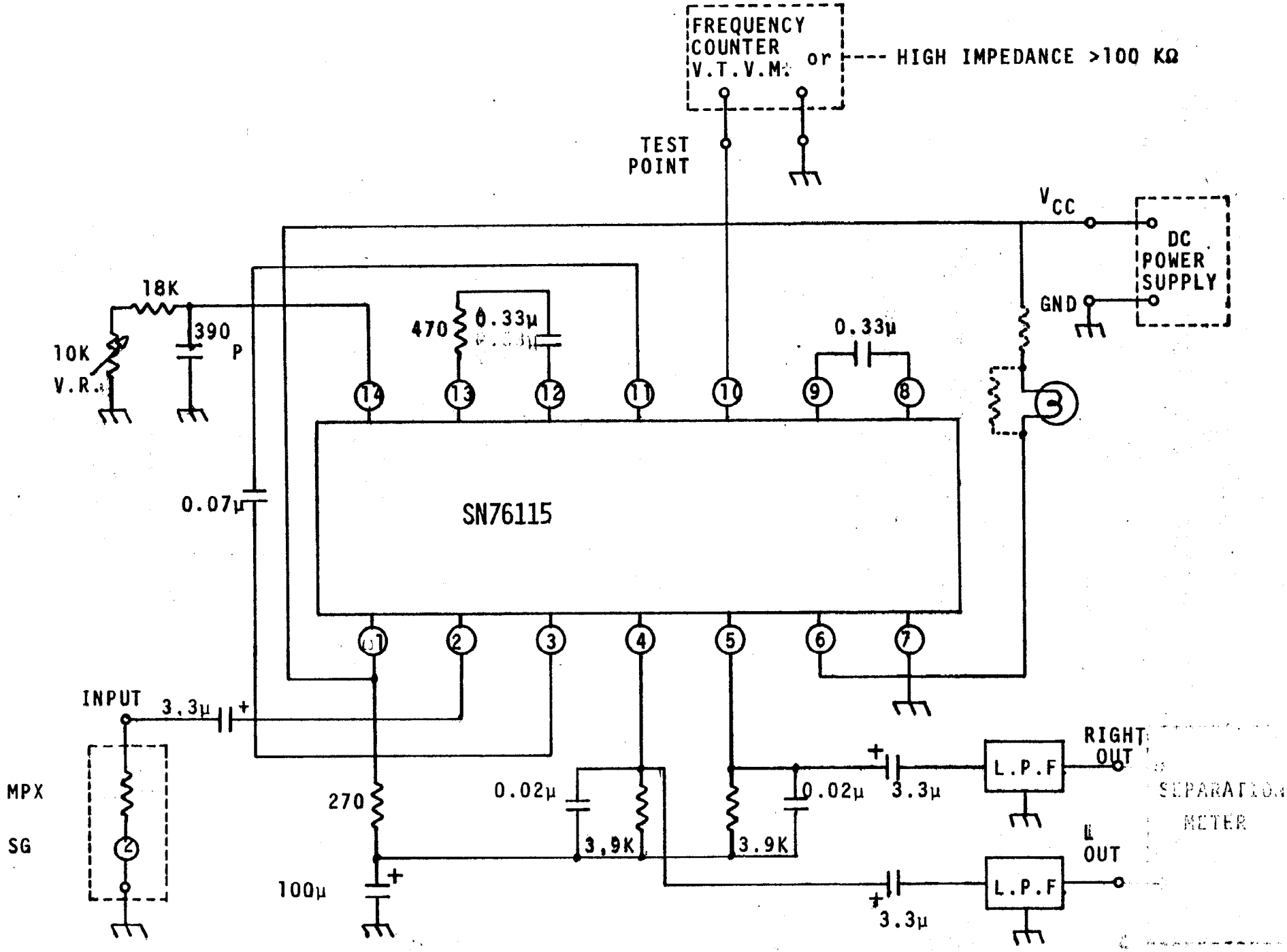
The circuit is so designed that phase lag may be generated by adding a capacitor from pin 3 to ground. The source resistance at this point is 500 ohms. A capacitance of 820 pF compensates the 5.5^{o} phase lead : increase above this value causes the regenerated sub carrier to lag the original.

Note that these phase shifts occur within the phase lock loop and affect only the regenerated 38kHz sub carrier: the circuit causes no significant phase or amplitude variation in the actual stereo signal prior to decoding.

Voltage Control Oscillator Compensation Figure 3 illustrates uncompensated Oscillator Drift versus temperature. The recommended T_C of the R_4,R_5,C_7 combination is -200ppm. This will hold the oscillator drift to approximately ±0.5% over a temperature range of -30 to $+85^{o}$c. Acceptable performance is obtained with up to 2.5% oscillator detuning, which with the compensation given above, allows ±2% for aging of the timing components.

FIGURE 3




FREQUENCY COUNTER V.T.V.M.
or
HIGH IMPEDANCE >100 KΩ
TEST POINT
V_{CC}
DC POWER SUPPLY
GND
18K
10K V.R.
390 P
470
0.33μ
0.33μ
0.07μ
SN76115
INPUT
3.3μ
MPX
SG
270
100μ
0.02μ
3.9K
3.9K
0.02μ
3.3μ
3.3μ
L.P.F
L.P.F
RIGHT OUT
L OUT
SEPARATION METER